REMARKS

Present Status of the Application

Claims 1-5 and 7-14 are pending in the above-identified application. The Final Office Action dated June 3, 2002 rejected claims 1, 5, 7 and 11-13 under 35 USC 103(a) as being unpatentable over Lach et al. (US Patent No. 6,108,212). Claims 2-4, 8-10 and 14 were rejected under 35 USC 103(a) as being unpatentable over the same Lach et al. in view of the admitted prior art (APA). Claims 4 and 10 were rejected under 35 USC 103(a) as being unpatentable over Lach et al. and APA in view of Katchmar (US Patent No. 6,194,782). Claim 1 was objected to because of minor language informalities.

The Applicants have most respectfully considered the remarks set forth in the Final Office Action. Regarding the obviousness issues raised under 35 USC 103(a), it is however strongly believed that the cited references are deficient to adequately teach the claimed invention. To provide a clearer description of the claimed invention, the language of claims 1 and 7 has been amended in this response without introduction of additional limitations. Furthermore, claims 2 and 8 have been amended to withdraw minor typographic errors. It is submitted that no new matters have been added in the amendments made herein. The reasons that motivate the above position of the Applicants with respect to the obviousness rejections are discussed in detail hereafter, upon which reconsideration and allowance of the claims are most earnestly solicited.

Discussion of the Office Action Rejections

Discussion of the claim rejection under 35 USC 103

1. The Office Action rejected claims 1, 5-7 and 11-13 under 35 USC 103(a) as being allegedly

unpatentable over Lach et al.. This rejection is respectfully traversed.

As stated in the MPEP §2143, to establish a prima facie case of obviousness, three basic requirements must be met. First, some suggestion or motivation must be found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the references or to combine the reference teachings. Second, success must be reasonably expected. Finally, the cited reference (or references when combined) must teach or suggest all the claim limitations. The Applicants traverse the rejection because the standard for a proper rejection on the grounds of prima facie case of obviousness as discussed in the MPEP has not been met.

As illustrated in FIG. 3 and FIG. 4 (and recited in amended claims 1 and 7), the claimed invention teaches a substrate structure of flip chip package in which a plurality of first and second mounting pads 214, 216 are defined on a top patterned circuit layer of the substrate. *A solder mask layer 222* covers the top patterned circuit layer *on the top surface of the substrate*, and further *partially covers a top surface 214a of the first mounting pads 214 while entirely exposing a second top surface 216a and sidewalls 216b of the second mounting pads 216.* The *first and second mounting pads 214, 216* constructed according to the above manner *are respectively arranged at a peripheral region and a central region of the substrate.* As disclosed on page 8 of the specification, the above substrate structure has the advantages of no-void filling of an underfill material between the substrate and a chip mounted thereon, and good bonding of conductive bumps to the mounting pads.

In connection to the arguments set forth in the previous response to Office Action, the Applicants respectfully re-assert that Lach et al. wholly fails to disclose and suggest the claimed

invention in which the solder mask, the first and second mounting pads are disposed in the manner reported above.

Lach et al. discloses a surface-mount device package in which at least an integral resistor 32 is formed from the electrical connection of a resistive volume 36 to both a component pad 27 and a terminal 34 on a lower surface of an interposer 14 (see FIG. 1 and col. 3, lines 26-39). The resistive volume 36 may be outwardly covered with a solder mask 42 (see FIG. 2). The resistive volume 36 partially covers the component pad 27 so that a conductive bump 28 can be electrically attached to the exposed region of the component pad 27.

It first should be noted that the above reported disclosure of Lach et al., in contrast to the claimed invention, is completely silent about the presence of *any patterned circuit layers* included in the substrate/interposer. This deficiency cannot be ignored. As illustrated, Lach et al. further only teaches that the solder mask 42 covers the resistive volume 36, which clearly does not meet the features of the claimed invention in which *the solder mask layer should cover the top patterned circuit layer on the top surface of the substrate.* This limitation missing in Lach et al. is explicitly recited in amended claims 1 and 7 that therefore patently distinguish over Lach.

The Examiner further asserts that Lach et al., as shown in FIG. 6 and FIG. 8, discloses the first mounting pads are disposed at the peripheral region of the substrate while the second mounting pads are disposed at the central region of the substrate similar to the claimed invention.

The Applicants strongly disagree with the above assertion of the Examiner. FIG. 6 and FIG. 8 of Lach et al. are local planar views of the interposer representing in details the structure of the integral resistor assemblies formed thereon (see col. 7, lines 19-36). These views clearly do not show *any solder mask layer covering the top patterned circuit layer on the top surface of*

the substrate as discussed above. These views further do not illustrate any *solder mask layer partially covering the first top surface of the first mounting pads at the peripheral region of the substrate*, while *entirely exposing the second top surface and sidewalls of the second mounting pads at the central region of the substrate*. It is believed that one person skilled in the art would readily understand that the claim wording "peripheral region" means a region of the substrate that is out of the "central region" of the substrate, which is clearly not described nor suggested in the cited reference.

In addition to the absence of a solder mask layer disposed in the manner claimed, it should be further noted Lach et al. explicitly suggests that the conductive bumps should be attached strictly on the top surface of the pads 26, 27 (see FIG. 1). This illustration clearly shows that Lach et al. is not concerned about good bonding characteristics of the conductive bumps with the pads 26, 27. The above fact raises the questions of motivation for combination alleged in the Office Action. As stated in *In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998)*, "the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select elements from the cited prior art reference for combination in the manner claimed".

For at least the above reasons, it is therefore submitted that Lach et al. wholly fails to adequately teach and suggest the claimed invention as recited in claims 1 and 7, and the withdrawal of the rejection is therefore respectfully requested.

2. The Office Action rejected claims 2-4, 8-10 and 14 under 35 USC 103(a) as being allegedly unpatentable over Lach et al. in view of the APA. This rejection is respectfully traversed.

Lach et al. is as discussed above.

It is further submitted that the APA exhibits at least the same deficiencies as Lach et al. discussed above. By virtue of their dependency upon patentable independent claims 1 and 7, the Applicants therefore submit that claims 2-4, 8-10 and 14 should be also patentable over the prior art.

3. The Office Action rejected claims 4 and 10 under 35 USC 103(a) as being allegedly unpatentable over Lach et al. and the APA as above, and further in view of Katchmar. This rejection is respectfully traversed.

Although Katchmar may disclose a semiconductor package in which ball pads/solder balls 40 in a central region of the substrate have a pitch smaller than that of ball pads at the peripheral region of the substrate, Katchmar however exhibits the same deficiencies as Lach et al. and the APA. Like Lach and the APA, Katchmar at least fails to teach and suggest the disposition of the solder mask layer and first and second mounting pads as recited in independent claims 1 and 7 and discussed above. By virtue of their respective dependency upon the patentable independent claims 1 and 7, it is therefore submitted that claims 4 and 10 should be also patentable over the cited references. The withdrawal of the rejection is therefore respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-5 and 7-14 of the present application patently define over the prior art and are in proper condition for

allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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VERSION WITH MARKED-UP AMENDMENTS TO SHOW THE CHANGES MADE

In The Claims

Please amend the claims as follows.

1. (Twice amended) A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layers;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip-chip package as a top patterned circuit layer, and the top patterned circuit layer comprises at least a plurality of [a] first mounting pads and a plurality of [a] second mounting pads; and

a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package, the solder mask layer partially covering a [portion of the surface on the outer edge] first top surface of the first mounting pads [and a side surface of the first mounting pad] while entirely exposing [a portion of the surface of the first mounting pad and the whole] a second top surface and sidewalls of the second mounting pads, wherein the first mounting pads are disposed [on the] at a peripheral region of the substrate and the second mounting pads are disposed at a central region of the substrate.

2. (Once amended) The substrate structure of Flip Chip package of claim 1 wherein the material for the insulative layer is selected from the group consisting of ["] flame-retardant epoxy-glass fabric composite resin["], [Bismaleimide-Taiazine] Bismaleimide-Triazine (BT), and epoxy.

7. (Twice amended) A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layer;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package as a top patterned circuit layer, and the top patterned circuit layer comprises at least a plurality of [a]first mounting pads and a plurality of [a] second mounting pads;

a solder mask layer covering the top patterned circuit layer on the surface of the substrate of the flip chip package, [and] the solder mask layer partially covering a [portion of the surface on the outer edge] first top surface of the first mounting pads while entirely exposing [a portion of the surface of the first mounting pad and the whole] a second top surface and sidewalls of the second mounting pads, wherein the first mounting pads are formed at [the] a peripheral region of the substrate;

a chip having an active surface with a plurality of bumps disposed thereon wherein the chip has its active surface face to the surface of the substrate of the flip chip package, and the bumps are electrically connected to their corresponding first bonding pads and second bonding pads respectively; and

an underfill material filling between the active surface of the chip and the top surface of the substrate of the flip chip package.

8. (Once amended) The substrate structure of Flip Chip package of claim 7 wherein the material for the insulative layer is selected from the group consisting of ["]flame-retardant

epoxy-glass fabric composite resin["], [Bismaleimide-Taiazine] Bismaleimide-Triazine (BT), and epoxy.